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PAPER

A facile route for the fabrication of large-scale gate-all-around nanofluidic field-effect transistors with low leakage current†

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Active modulation of ions and molecules *via* field-effect gating in nanofluidic channels is a crucial technology for various promising applications such as DNA sequencing, drug delivery, desalination, and energy conversion. Developing a rapid and facile fabrication method for ionic field-effect transistors (FET) over a large area may offer exciting opportunities for both fundamental research and innovative applications. Here, we report a rapid, cost-effective route for the fabrication of large-scale nanofluidic field-effect transistors using a simple, lithography-free two-step fabrication process that consists of sputtering and barrier-type anodization. A robust alumina gate dielectric layer, which is formed by anodizing sputtered aluminium, can be rapidly fabricated in the order of minutes. When anodizing aluminium, we employ a hemispherical counter electrode in order to give a uniform electric field that encompasses the whole sputtered aluminium layer which has high surface roughness. In consequence, a well-defined thin layer of alumina with perfect step coverage is formed on a highly rough aluminium surface. A gate-all-around nanofluidic FET with a leak-free gate dielectric exhibits outstanding gating performance despite a large channel size. The thin and robust anodized alumina gate dielectric plays a crucial role in achieving such excellent capacitive coupling. The combination of a gate-all-around structure with a leak-free gate dielectric over a large area could yield breakthroughs in areas ranging from biotechnology to energy and environmental applications.

Introduction

Nanofluidics has received considerable interest during the last decade for implementing its unique features to various state-of-the-art technological applications such as DNA sequencing,[1] single-biomolecule sensing,[2] protein control,[3] desalination,[4] energy conversion,[5] *etc.* A keyword defining nanofluidics is the Debye screening length, which represents the characteristic length at which the surface potential (or zeta potential) deviates from the bulk electrolyte because of the electric double layer that forms on the solid–liquid interface.[6] In general, the Debye screening length is on the order of 1 to 100 nm, depending on the ionic strength of the electrolyte.[3] When one or more dimensions of the channels are comparable to or smaller than this scale, the electric potential of the bulk electrolyte is influenced by the surface potential, and subsequently dominates the transport behavior. The influence of this potential allows for the unique manipulation of ions and biomolecules. Nanofluidic diodes[7–10] and transistors[11–18] are typical examples of manipulating ions and biomolecules that are enabled by the surface-governed features of nanofluidics.

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The surface potential can be actively manipulated by introducing a field-effect control that modulates the surface potential through capacitive coupling at the surface of the channel. This is essentially a gating action in a metal-oxide-semiconductor field-effect transistor (MOSFET). In order to perform a strong capacitive coupling that provides excellent gating, there are several conditions to be met. First, the gate dielectric should be as thin as possible without suffering dielectric breakdown in order to maximize the capacitance of the gate dielectric. Also, the gate dielectric should be well-defined, that is free from pinholes or defects. However, these are somewhat contradictory because, obviously, as the gate dielectric becomes thinner the chance of having pinholes and tunneling current increases, which leads to gate leakage.

Gate leakage is an important aspect of implementing a FET device.[19] In nanofluidic FETs, the gate leakage limits the gating performance of FET and degrades its robustness. Also, it is known that gate leakage can hydrolyze water to generate either H_3O^+ or OH^- ions that alter the pH of the electrolyte which directly influences the gating performance by changing the charge and chemistry of the dielectric surface.[20]

Furthermore, besides thin and good-insulating gate dielectric, an ideal gate is capable of applying electric field along the whole perimeter of the channel, which makes the gate-all-around structure ideal for field-effect control.[21] For a nanofluidic FET, a gate-all-around structure can generally be achieved by forming a

gate and gate dielectric on top of a porous substrate.[13–17] However, it is extremely challenging to fabricate a well-defined gate dielectric for the all-around gate structure because the gate metal exhibits high curvature and roughness, especially for the vertical sidewall region at the pore entrance. Therefore, a method with perfect step coverage is required in order to achieve a leak-free gate dielectric on an all-around gate structure. Conventional deposition methods that are known to exhibit good step coverage such as sputtering and chemical vapor deposition (CVD) are unsatisfactory. Up to date, atomic layer deposition (ALD) was the only solution for creating a good gate dielectric on an all-around gate structure.[13,15] However, ALD is a time-consuming technique that does not meet the criteria of needs for rapid fabrication.

In this paper, we present a facile route for the fabrication of leak-free, gate-all-around nanofluidic FETs over a large area by employing a simple two-step fabrication process that consists of sputtering and anodization for forming the gate metal and gate dielectric, respectively. These fabrication processes are well-defined, cost-effective, feasible, and rapid. We show that the barrier-type anodizing technique gives an outstanding insulation performance with a minimal dielectric thickness, which suggests an ideal way of fabricating gate dielectrics in a nanofluidic FET. The combination of a gate-all-around structure with a leak-free gate dielectric over a large area yields an excellent gating performance despite the relatively large channel size.

Experimental

A schematic of the two-step fabrication process for the nanofluidic FET is illustrated in Fig. 1(a). The nanofluidic FET was fabricated by starting with a porous supporting membrane that was to form the base pore structure. A commercially available porous alumina membrane, Anodisc® (nominal pore diameter 200 nm) was employed. Fig. 1(b) and (d) show the scanning electron microscope (SEM) images of both the top and cross-section, respectively, of the porous membrane, which has an average pore diameter of approximately 320 nm.[22,23] On this side of the membrane, 300 nm of aluminium was sputtered (SME-200E, ULVAC) to form the gate metal layer. Consequently, the pores were narrowed (Fig. 1(c) and (e)) to an average open size of approximately 27.9 nm based on the Gaussian fit (Fig. 1(f)). The pore density was estimated to be about 1–1.5 $\times$ 10^9 cm^{-2}.

Subsequently, in order to form a gate dielectric layer, a barrier-type anodization was performed over an area of about 30 mm^2. The procedure for barrier-type anodization of aluminium was adopted from previous literature reports based on 0.1 M borate solution (ammonium pentaborate octahydrate, Sigma-Aldrich).[24–27] Prior to anodization, the membrane was immersed in the borate solution and left in a vacuum chamber in order to remove any trapped air bubbles from the pores and fully wet the membrane and aluminium layers. Initially, a constant current density was applied until the voltage had reached the desired level, which was 10 and 6.15 V for this study. The previous literature reports that a 1 mA cm^{-2} of initial current is generally applied to thin film samples and results in a linear voltage increase at a rate of approximately 0.4–0.5 V s^{-1}.[26,27] However, this cannot be directly adapted to this study because of the enlarged surface area of sputtered aluminium due to the highly curved surface. Therefore, the initial current density was corrected to 3 mA cm^{-2} based on the projected area, which

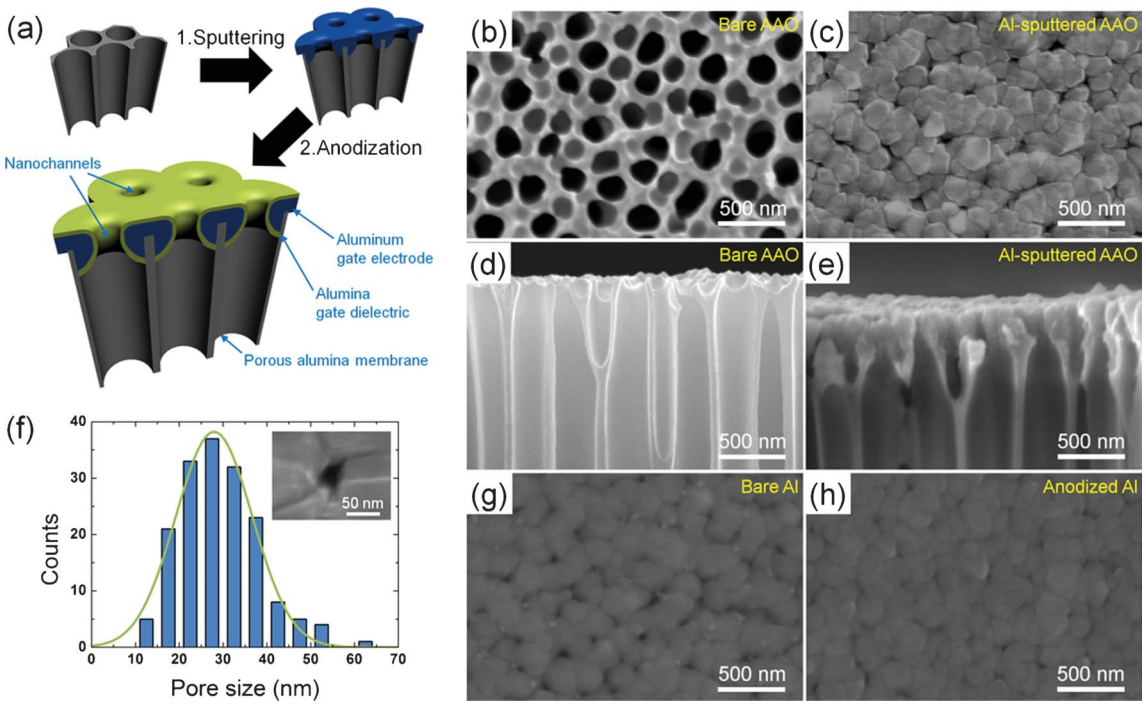

Fig. 1 The two-step fabricated nanofluidic FET: (a) Schematic of the two-step fabrication process; (b) Top and (d) cross-sectional SEM images of bare Anodisc® membrane; (c) Top and (e) cross-sectional SEM images of aluminium sputtered Anodisc® membrane; (f) Size distribution of the aluminium-sputtered nanopores. Gaussian fit gives a mean value of 27.9 nm. Inset is a magnified SEM image of a typical aluminium-sputtered nanopore; SEM images of (g) bare and (h) anodized aluminium surface from the same sample.

exhibited a voltage rise rate of approximately 0.4 V s^{-1}. The limiting anodizing voltage, V_a, was set to 10 and 6.15 V for this study in order to form two different thicknesses.[24] Subsequently, the voltage was held for several minutes until the current was dropped down to 1% of the initial value. This holding step was important in reducing pinholes and defects, and forming a robust alumina layer.[28] A commercial potentiostat (VersaSTAT3, Princeton Applied Research) was employed for the anodization process.

Furthermore, to promote the uniform formation of the anodized alumina layer on the rough, curved surface of the aluminium layer, we artificially modified the counter electrode for the anodizing experiment. Instead of using planar, wire, or cylinder-type counter electrodes, which are generally used in electrochemistry experiments, we utilized a hemispherical concave electrode in order to provide a uniform electric field spread along the roughly curved aluminium surface. In principle, anodized alumina is formed by the migration of mobile aluminium cations and oxygen anions in a direction normal to the applied electric field.[24] Unlike planar thin films, the sputtered aluminium layer in this study exhibits very rough and convex structures (Fig. 1(e)), which may hinder the migration of mobile aluminium cations towards the solid–electrolyte interface because of distortions in the electric field. This effect is especially strong for the aluminium layers located at the bottleneck of the pores that are formed by the high step coverage of sputtering. Therefore, to mitigate this problem by providing a uniform electric field along the aluminium surface including the bottom edge of the aluminium layer, we employed a hemispherical concave counter electrode that encompasses the whole aluminium layer for the anodization process.

To observe the structural features of the nanofluidic FET, SEM (S-4300, Hitachi) and TEM (JEM-2100F, JEOL) imaging were conducted. TEM samples were prepared using the focused ion-beam (FIB; Helios NanoLab, FEI) technique (Fig. S1 in ESI†).

After anodizing, the membrane was placed between two KCl reservoirs in order to characterize the ionic transport behavior (Fig. S2 in ESI†). A silicone rubber gasket was used in order to prevent KCl leakage. For gate leakage characterization, a voltage sweep between the gate electrode and Ag/AgCl electrode immersed in the reservoir of 10^{-4} M KCl at the gate side was performed under a voltage range of ± 2 V at a scan rate of 100 mV s^{-1}.

For channel conductance measurement, ionic current was monitored for 1 min in order to reach steady-state. Channel bias was from 0 to 1 V with steps of 200 mV. Gating experiments were done under 10^{-4} M KCl electrolyte. The gate voltage was applied from 2 to -2 V with a step of 400 mV. The voltage sweep and I–V measurements were performed using the same potentiostat that was used in anodization process whereas the gate potential was applied by a function generator (33210A, Agilent). All electrical measurements were conducted inside a Faraday cage.

Results and discussion

Fig. 2 shows the transmission electron microscope (TEM) images of the cross-section of the gate structure formed under different

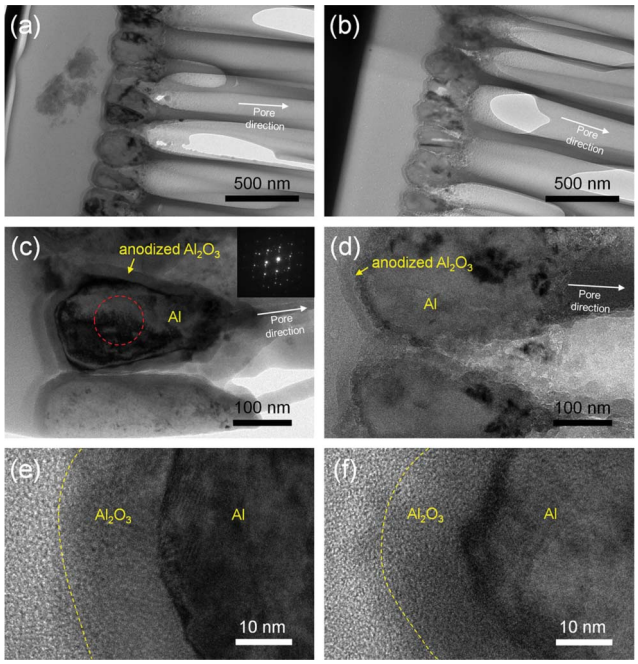

Fig. 2 TEM images of the nanofluidic FET for two different V_a conditions: (a), (c), (e) V_a = 10 V; (b), (d), (f) V_a = 6.15 V. Inset of (c) is the electron diffraction pattern for the selected area of the aluminium (red dashed box). The electron diffraction pattern in the inset of (c) and lattice fringes in (e) and (f) indicate the clear presence of a single crystalline aluminium layer.

anodizing conditions, *i.e.* V_a = 10 and 6.15 V. It is clearly shown that a uniform, well-defined alumina layer is formed along the perimeters of the curved aluminium layer. No significant image contrast was observed in the anodized alumina layer, which implies the formation of a robust, defect-free dielectric layer. The results of both elemental mapping, shown in Fig. 3, and energy dispersive spectroscopy (EDS), found in the ESI† (Fig. S3 in ESI†), further confirm the uniform formation of alumina with perfect step coverage. It is remarkable that a uniform dielectric layer can be formed on such a rough, curved surface in a short period of time of several minutes with a minimum cost, which no other conventional deposition method can achieve.

From the high-resolution TEM images in Fig. 2(e) and (f), the thicknesses of two different V_a conditions are determined to be approximately 20 and 15 nm for V_a of 10 and 6.15 V, respectively. This result agrees with previous reports on thin film samples where it is well-known that the thickness of the anodized aluminium depends on the final anodizing voltage.[24–27] In a borate solution, the thickness and the anodizing voltage have the following relationship: $t = 1.3V_a + 2$ where t is the thickness of the anodized alumina in nanometres.[24–27] This corresponds to 15 and 10 nm thick alumina layers for V_a of 10 and 6.15 V, respectively, which leads to the conclusion that when the concave electrode is used, neither the curvature or roughness significantly affects the thickness of the anodized alumina.

It should be noted that when anodized, a considerable amount of volume expansion occurs because the anions are incorporated into the aluminium films;[28] this volume change should affect the size of the pores. A simple quantitative analysis of this volumetric change in the alumina leads to approximately 10.4

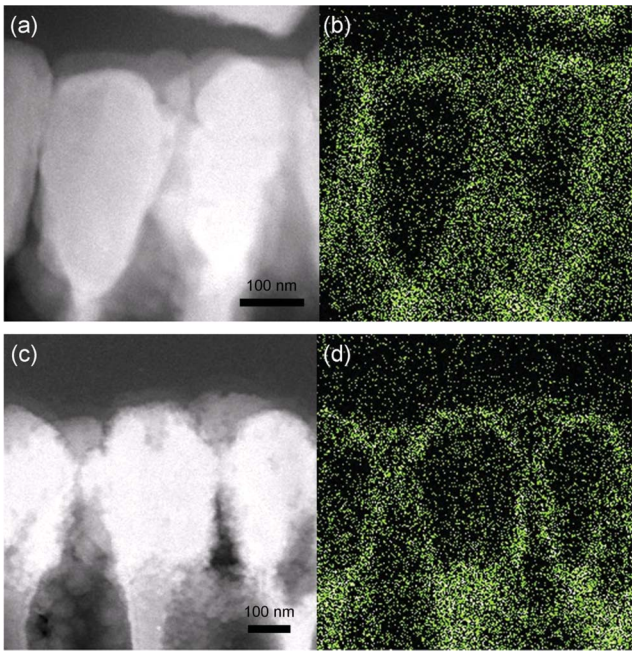

Fig. 3 Scanning TEM images and the corresponding oxygen element maps of the nanofluidic FET for two different V_a conditions: (a), (b) V_a = 10 V; (c), (d) V_a = 6.15 V.

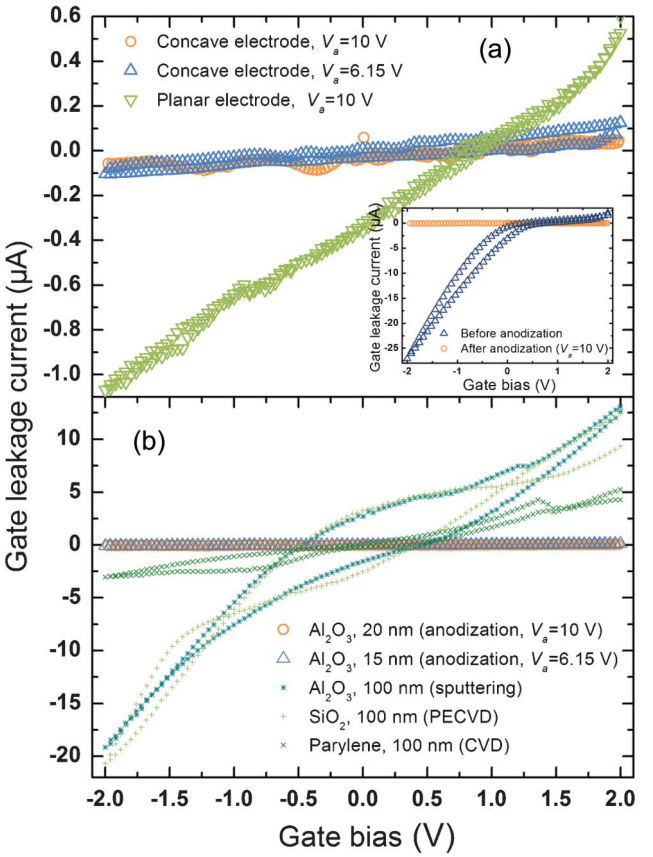

Fig. 4 Gate leakage characterization *via* cyclic voltammetry between the gate and Ag/AgCl electrode in 10^{-4} M KCl. (a) Cyclic voltammetry results for different electrodes used during anodization. Orange and blue symbols represent experiments using a concave electrode with a V_a of 10 V (thickness = 20 nm) and 6.15 V (15 nm), respectively, whereas the green symbol represent the planar electrode with V_a of 10 V. Inset shows the cyclic voltammetry results from before and after anodizing with a concave electrode at V_a = 10 V. (b) Cyclic voltammetry results for various types of gate dielectric layer.

and 7.8 nm of size change in the pores of alumina for V_a of 10 and 6.15 V, respectively (see ESI† for detailed derivation). Fig. 1(g) and (h) show the SEM images for comparing the effect of anodization on the pore sizes. The two images are both from the same sample where the area of non-anodized layer is obtained by removing the mask layer. These images show that the pores are further shrunk by anodization because of the volume expansion in the alumina layer. Therefore, we determined the effective average pore sizes for V_a of 10 and 6.15 V after anodization as 17.5 and 20.1 nm, respectively, by subtracting the pore size change from the average pore size (27.9 nm).

With these strategies, a robust, leak-free gate dielectric was successfully obtained. We characterized the insulating performance of anodized alumina gate dielectric by conducting cyclic voltammetry between the aluminium gate and Ag/AgCl counter electrode in 10^{-4} M KCl electrolyte (Fig. 4). The voltage was swept from 2 to −2 V with a scan rate of 0.1 V s^{-1}. Obviously, the gate leakage was significantly decreased after the anodization process (inset of Fig. 4(a)). It is also shown from Fig. 4(a) that by use of the concave electrode, we have further reduced the gate leakage, which was most likely caused by the well-defined anodized alumina at the pore bottleneck region. No sign of current rise due to the leakage current was observed in the experimental range. We sometimes observed devices exhibiting no gate leakage even at 5 V. However, as the insulating performance for voltages greater than ±3 V varied from device to device, we set the gate voltage in the reliably insulating range, from 2 to −2 V.

We also compared the gate leakage behavior to the conventional passivation methods having high step coverage, such as chemical vapor deposition (CVD) and sputtering (Fig. 4(b)). 100 nm of silica, alumina, and parylene were formed by plasma-enhanced CVD (PECVD), sputtering, and parylene coater, respectively (detailed explanations can be found in the ESI†). Amazingly, the anodized alumina exhibited an exceptional insulation performance compared to these conventional methods despite having several factors smaller thickness. We attribute this to the forming environment of the anodization process. Unlike other passivation techniques, anodization is conducted in a liquid environment. This provides an ideal way of forming a passivation layer under a similar environment for implementing a nanofluidic FET, *i.e.*, aqueous.

In order to obtain the surface charge of the nanochannels and to seek for the possibility as a nanofluidic FET, the concentration-dependent channel conductance was measured. Two Ag/AgCl electrodes were placed across the membrane and subsequently the ionic current was measured. Fig. 5 shows the measured channel conductance under various KCl concentrations. The data shows a typical conductance plateau at low KCl concentrations because the primary mechanism of ionic transport has changed from geometry-governed ion transport to surface charge-governed ion transport.[6,29,30] The critical point where the transition of the curve is initiated is called the critical

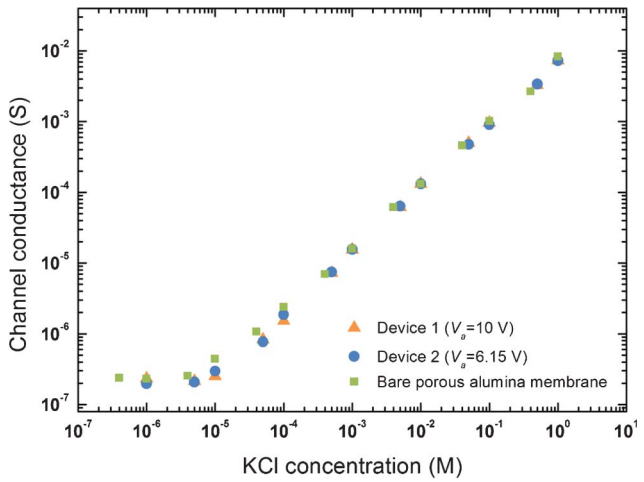

Fig. 5 Concentration-dependent channel conductance. Orange triangles and blue circles represent the results from devices with V_a of 10 and 6.15 V, respectively, whereas green squares represent the results from bare porous alumina membrane.

concentration, C_{cr}. This value corresponds to a certain point where the two ion transport mechanisms are identically responsible for the ion transport. Under this concentration, the total number of the ions occupied in the nanochannel is equal to the total surface charge of the channel. The geometry of the nanochannel for this study can be simply modeled as two cylinders connected coaxially where one cylinder corresponds to the narrow and short channel at the gate part and the other cylinder corresponds to the porous alumina membrane which exhibits relatively wide and long channels. Therefore, the equation for the charge equilibrium at C_{cr} can be expressed as follows:

$$(2\pi r_1 l_1 + 2\pi r_2 l_2)\sigma = (\pi r_1^2 l_1 + \pi r_2^2 l_2)FC_{cr} \quad (1)$$

where r and l are the radius and the length of the cylindrical nanochannel, respectively, σ is the surface charge, and F is the Faraday constant. The left term represents the total surface charge of the nanochannel whereas the right term represents the total number of ions inside the nanochannel. The subscripts 1 and 2 correspond to the narrow and wide nanochannels, respectively. As can be clearly seen from Fig. 1 and 2, the length and the width of the nanochannel at the gate structure is significantly small compared to the nanochannel at the porous alumina membrane. Therefore, the terms regarding subscript 1 in eqn (1) can be neglected, and the resulting surface charge can be approximated as follows.

$$\sigma = \frac{FC_{cr}r_2}{2} \quad (2)$$

This approximation is further confirmed by additional channel conductance experiment on a bare porous alumina membrane (green squares in Fig. 5) where the existence of the gate structure does not critically affect C_{cr}. Regarding C_{cr} as 4×10^{-5} M from Fig. 5 and r_2 as 160 nm from the previously measured data,[23] the surface charge of the anodized alumina is estimated as 0.31 mC m^{-2}. This value is about an order lower compared to the previous reports where the surface charge of anodized alumina was reported as about 2–5 mC m^{-2}.[28,31] This low surface charge of the anodized alumina, which is favorable for implementing the field-effect modulation of ions,[11] may be attributed to the unique surface chemistry of the metal oxide in an aqueous environment. When in contact with water, the surface chemistry of the oxide is governed by simultaneous protonation and deprotonation of hydroxyl groups that is sensitive to the pH.[32] For instance, protonation of the hydroxyl group is pronounced when the pH is low whereas deprotonation governs when the pH is high. Obviously, there exists an intermediate value, termed the point of zero charge (pzc), where the net surface charge is zero due to the balance between protonation and deprotonation. The pzc of alumina is known as about pH = 5–8,[10,15,32] which is near neutral. Because the electrolyte used in this study was neutral and no pH buffers were added, the surface charge of the alumina should be small enough. This low effective surface charge has thus resulted in the low transition point, C_{cr}, compared to other studies such as silica (pzc of silica is pH = 1–2).[11,12,29,30,34] Note that a recent report by Jiang and Stein has shown that the surface charge of the alumina grown by ALD can reach up to more than 25 mC m^{-2} at pH = 3.[15]

Finally, we have investigated the gating behavior of the nanofluidic FET by measuring the channel conductance as a function of the applied gate voltage. Fig. 6 shows the channel current at a 1 V bias under varying gate voltages in 10^{-4} M KCl electrolyte. The increase in the channel current under a negative gate voltage implies that the surface charge of the nanochannel is negative and the mobile ions are unipolar with cations being dominant, which is analogous to a p-type MOSFET.[12,13] The channel conductance increased up to a factor of 3.7 and 6.1 under a gate voltage of −2 V for devices with V_a of 10 and 6.15 V, respectively, which corresponds to an increased surface charge of 1.14 and 1.88 mC m^{-2}. This increased surface charge enhances the surface charge governed transport and eventually leads to an enhanced cation transport. However, under positive gate voltages, no significant change was observed. The reason for this asymmetric behavior, which was also frequently observed in the previous studies,[12–14] is not clear but it could possibly be due to the potential asymmetry from the intrinsic surface charge of

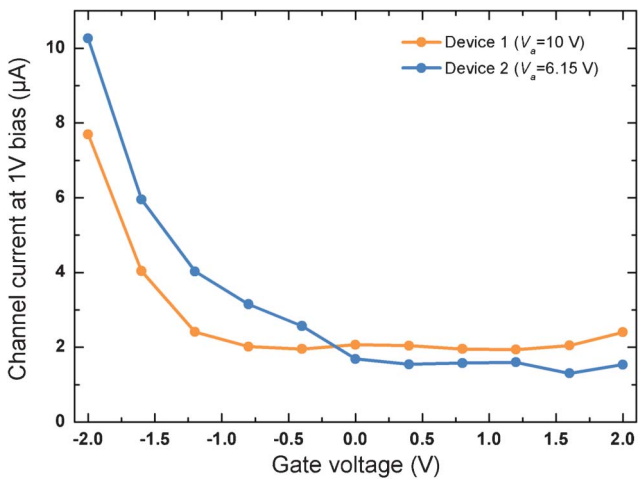

Fig. 6 Channel current at 1 V channel bias *vs.* gate voltage. Orange and blue lines represent results from devices with V_a of 10 and 6.15 V, respectively.

the alumina. Because the surface is negatively charged, increased surface charge under negative gate voltage attracts cations and thereby gives rise to the channel current. However, when the gate voltage is positive, up to a certain value, the surface charge is still negative because of the intrinsic surface charge of the alumina. Therefore, it is likely that a gate voltage of greater than 2 V is needed to deplete the cations and reduce the channel current. For instance, some previous reports showed that, under a large range of gate voltage, a monotonic conductance behavior was obtained.[11,17]

The transconductance to drain conductance ratio, which represents the effectiveness of the gating performance,[12,13] was calculated to be approximately 3.2 and 4.62 for the nanofluidic FETs with devices with V_a of 10 and 6.15 V, respectively. These values are much better than those from sub 10-nm pore nanofluidic FETs with planar gates[12] and comparable to 1 nm pore nanofluidic FET with gate-all-around structure.[13] In detail, Fan *et al.* showed the transconductance to drain conductance ratio of about 1.1 at 10^{-4} M electrolyte with mesoporous silica nanochannels (channel size $\sim$8 nm) that were gated with a top planar gate layer.[12] Compared to this value, our device showed several factors higher performance despite much larger channel size ($\sim$20 nm), which is attributed to the good capacitive coupling *via* the gate-all-around structure.

Comparing with the gate-all-around nanofluidic FET, Nam *et al.* reported that the highest transconductance to drain conductance ratio of a gate-all-around nanofluidic FET with 1 nm pores was estimated to be about 9.1 at 10^{-4} M electrolyte.[13] Regarding that the pore size presented in this study is more than an order larger, the performance is shown to be still competitive.

Also, the subthreshold swing is estimated as 1.55 and 1.43 V dec^{-1} for V_a = 10 and 6.15 V, respectively, which is much poorer than conventional MOSFETs ($\sim$70 mV dec^{-1}) but fairly comparable to silicon nanowire FETs (100–600 mV dec^{-1})[33,34] as well as 1 nm pore sized gate-all-around nanofluidic FET ($\sim$700 mV dec^{-1}).[13] These results are probably caused by the outstanding performance of the thin dielectric layer, which combines excellent capacitive coupling with minimal gate leakage. The good capacitive coupling for nanofluidic FET with thinner gate dielectric (15 nm) showed better gating performance compared to nanofluidic FET with relatively thicker gate dielectric (20 nm). The transconductance to drain conductance ratio as well as the subthreshold swing may be further enhanced when the electrolyte concentration is at the transition point, $C_{cr} = 4 \times 10^{-4}$ M, at which the gating effect for manipulating the overlap and non-overlap states of the electric double layer inside the nanochannels are more pronounced.[12,13]

Conclusion

In summary, we have achieved a competitive gating performance with a large-scale nanofluidic FET device that was fabricated *via* a simple two-step fabrication process consisting of sputtering and barrier-type anodization. A comprehensive list of features for various nanofluidic FETs including this study is summarized in Table S1 in the ESI.† The anodized alumina which was formed in just about several minutes exhibited excellent gate insulation performance with a minimal thickness. By forming a gate-all-around structure with a gate dielectric as thin as 15 nm, a good gating performance was demonstrated despite the relatively large pore size and low gate voltage. However, a more systematic study should be conducted in future studies that regards the optimal thickness of the anodized dielectric layer before deterioration because it is obvious that a thinner gate dielectric leads to much more pronounced capacitive coupling. Also, further in-depth studies regarding the electrokinetics should be conducted in order to deeply understand the fundamental mechanisms that are observed in this study. Nonetheless, our proposed nanofluidic FET can be easily fabricated over a large area, which suggests a possible utilization to various technological applications such as large-scale ion separation, desalination, power generation, drug delivery, and biomolecule manipulation.

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